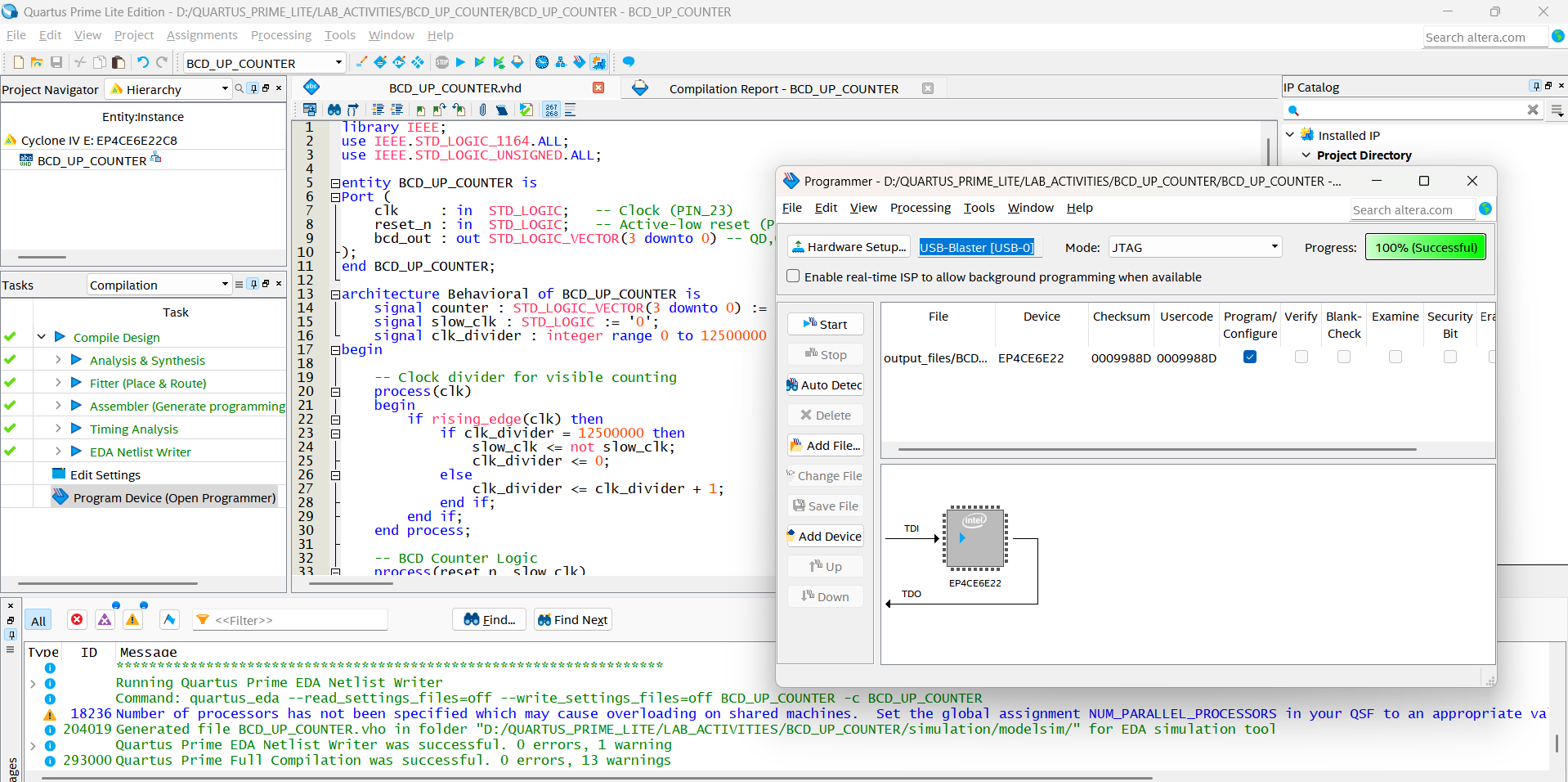
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C.Y.S.: BSCpE - 3A



**BCD UP COUNTER:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity BCD\_UP\_COUNTER is

Port (

clk : in STD\_LOGIC; -- Clock (PIN\_23)

reset\_n : in STD\_LOGIC; -- Active-low reset (PIN\_25)

bcd\_out : out STD\_LOGIC\_VECTOR(3 downto 0) -- QD,QC,QB,QA (MSB to LSB)

);

end BCD\_UP\_COUNTER;

architecture Behavioral of BCD\_UP\_COUNTER is

signal counter : STD\_LOGIC\_VECTOR(3 downto 0) := "0000";

signal slow\_clk : STD\_LOGIC := '0';

signal clk\_divider : integer range 0 to 12500000 := 0; -- 2Hz @ 50MHz

begin

-- Clock divider for visible counting

process(clk)

begin

if rising\_edge(clk) then

if clk\_divider = 12500000 then

slow\_clk <= not slow\_clk;

clk\_divider <= 0;

else

clk\_divider <= clk\_divider + 1;

end if;

end if;

end process;

-- BCD Counter Logic

process(reset\_n, slow\_clk)

begin

if reset\_n = '0' then

counter <= "0000"; -- Async reset

elsif rising\_edge(slow\_clk) then

if counter = "1001" then -- 9 in decimal

counter <= "0000"; -- Reset to 0

else

counter <= counter + 1; -- Increment

end if;

end if;

end process;

-- Active-low LED output (0=LED ON, 1=LED OFF)

bcd\_out <= not counter; -- Invert all bits

end Behavioral;

